

4.5.10 - 184 PIN UNBUFFERED DDR SDRAM DIMM FAMILY

CAPACITY--4M, 8M, 16M, 32M, 64M, 128M, & 256M WORDS OF 64, OR 72 BITS

DATA CONFIGURATIONS--Four DATA Word configurations are defined:

--64 BIT without PARITY

--72 BIT & 80 BIT for ECC CODES

CONFIGURATION--10 Different Configurations are defined using various combinations of X1, X4, X8, and X16 memories including 1 & 2 bank configurations, and three configurations for two asymmetrical banks.

LOGIC FEATURES--The modules contain a "SERIAL PRESENCE DETECT" feature that supplies encoded values that define the storage capacity, configuration, data word configuration, refresh mode, speed of the module and other characteristics and attributes of the module.

PACKAGE--184 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS--Figs. 4.5.10-A, & 4.5.10-B,

Summary of features and Pin Description--Figs. 4.5.10-C

SPD TABLE & INFORMATION--Fig. 4.5.10-D

Comparison of 184 Pin Unbuffered SDR SDRAM & DDR SDRAM DIMM--Fig. 4.5.10-E

KEYING METHODOLOGY--Fig. 4.5.10-F

VDDID Description--Fig. 4.5.10-G & 4.5.10-H

CONFIGURATION BLOCK DIAGRAM--Figs. 4.5.10-I through 4.5.10-P

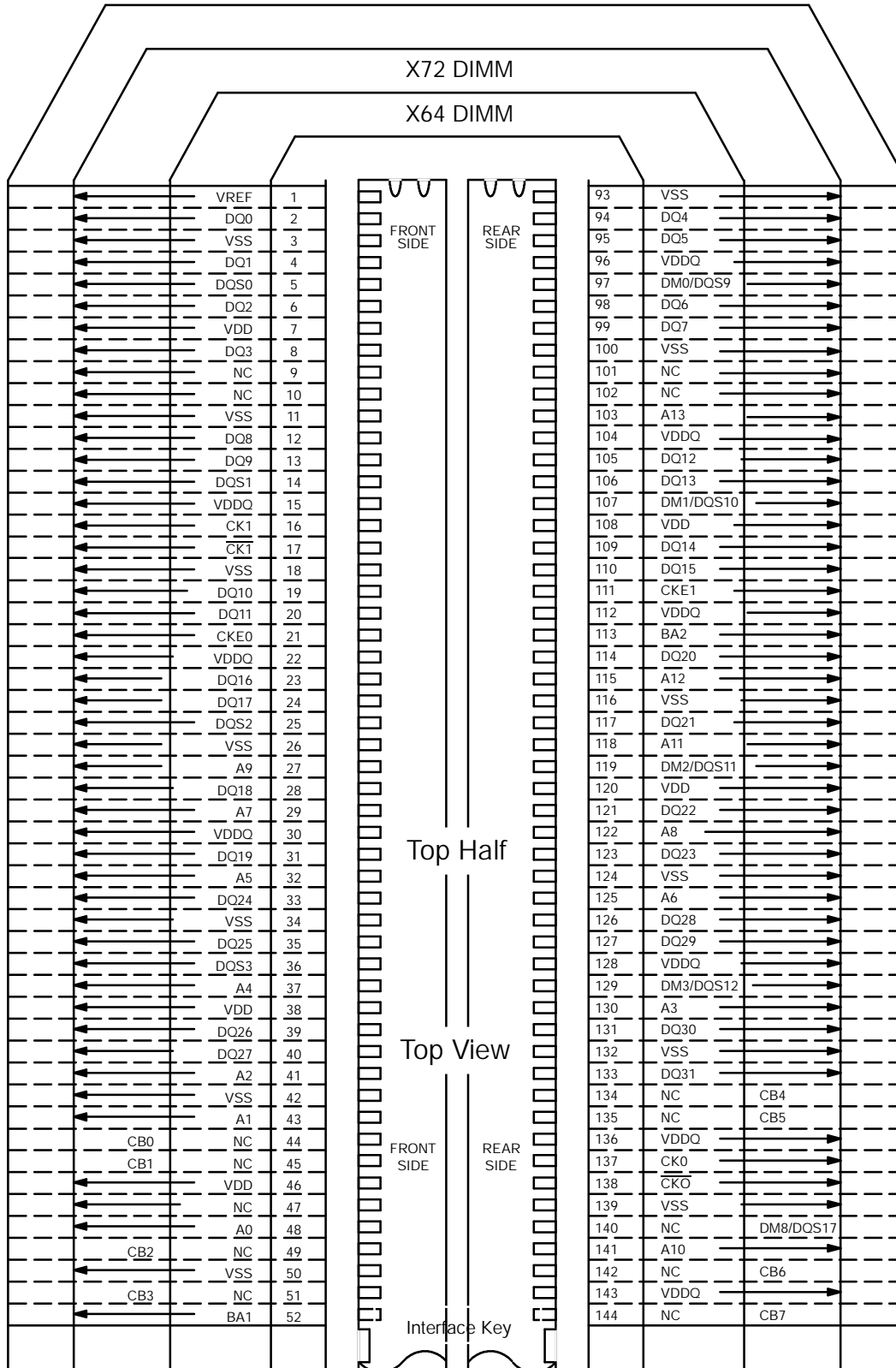


Figure 4.5.10-A
184 PIN, 64, OR 72 BIT DDR SDRAM DIMM PINOUT, TOP HALF

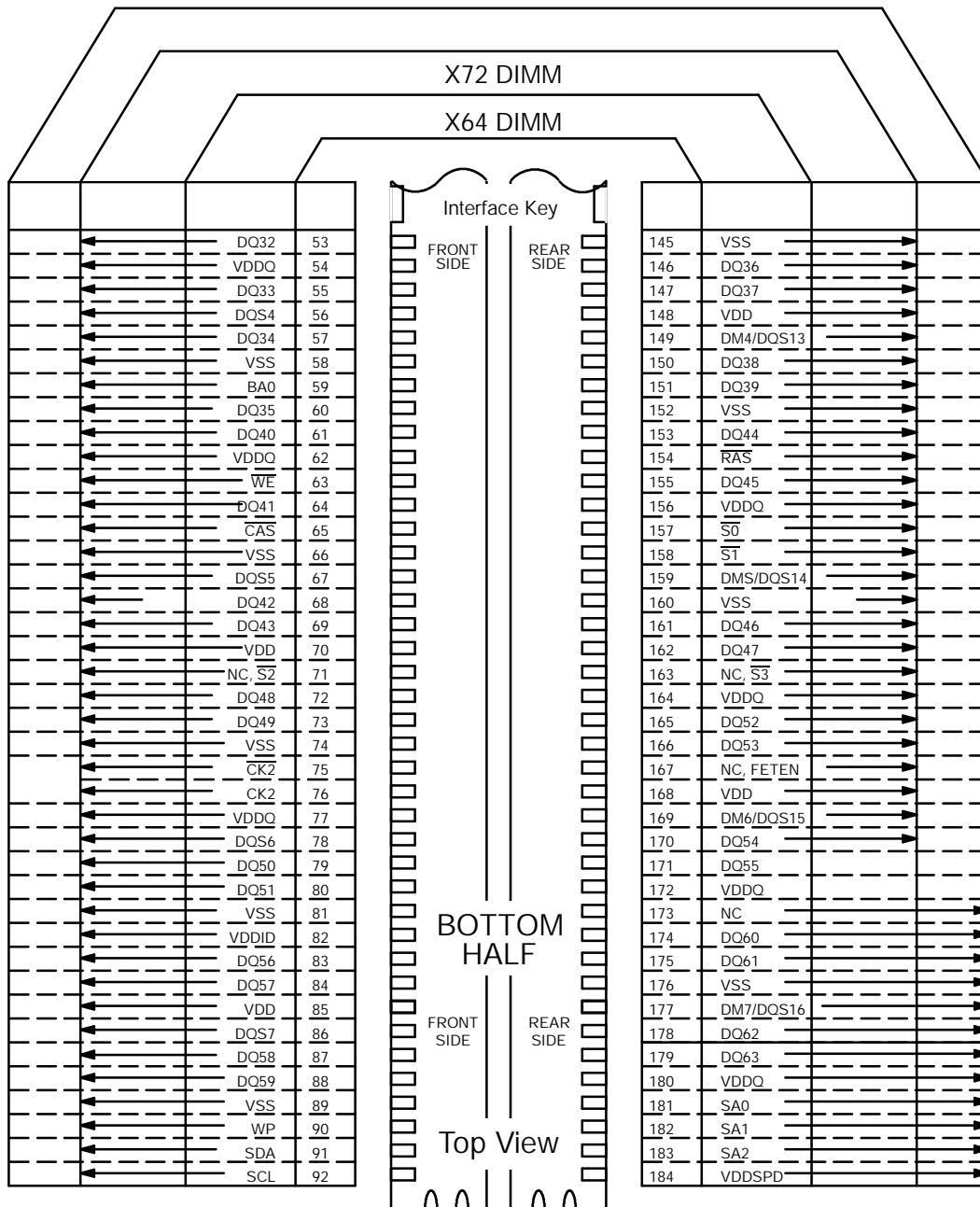


Figure 4.5.10-B

184 PIN, 64, OR 72 BIT DDR SDRAM DIMM PINOUT, BOTTOM HALF
Release 9

Features

DIMM Organization	x64, x72 ECC
DIMM Dimensions	5.25"L x 1 - 2"H x .157" / .354" thick (JEDEC Standard MO - xxx)
Pin Count	184 pins
SDRAMs Supported	64, 128, 256, 512Mb; 1Gb
Capacity	32MB - 2GB
Serial PD	2 wire interface (IIC)
Voltage Options	VDD/VDDQ: 3.3V/2.5V; 2.5V/2.5V; 2.5V/1.8V; 1.8V/1.8V; 1.8V/TBD
Interface	SSTL_2, TBD

Pin Description

Pin Name	# Pins	Description
A0 - A14	15	SDRAM address bus
BA0 - BA2	3	SDRAM bank select
DQ0 - DQ63	64	DIMM memory data bus
CB0 - CB7	8	DIMM ECC check bits
/RAS	1	SDRAM row address strobe
/CAS	1	SDRAM column address strobe
/WE	1	SDRAM write strobe
/S0 - /S1	2	SDRAM chip select lines (Phys. banks 0 and 1)
CKE0 - CKE1	2	SDRAM clock enable lines
DQS0 - DQS8	9	SDRAM low data strobes
DM(0-8)/DQS(9-17)	9	SDRAM low data masks/high data strobes (x4, 2 Phys. banks)
VDDID	1	VDD identification flag
CK0 - CK2	3	SDRAM clock (positive lines of 3 differential pairs)
/CK0 - /CK2	3	SDRAM clock (negative lines of these three pairs)
SCL	1	IIC serial bus clock for EEPROM
SDA	1	IIC serial bus data line for EEPROM
SA0 - SA2	3	IIC slave address select for EEPROM
WP	1	Write protect flag for EEPROM (Upper 128 bytes)
VDD	9	SDRAM positive power supply
VDDQ	16	SDRAM I/O Driver positive power supply
VREF	1	SDRAM I/O reference supply
VSS	22	Power supply return (ground)
VDDSPD	1	Serial EEPROM positive power supply
NC	4	Spare pins (no connect)
NC, /S2 - NC, /S3	2	Reserved pins (Phys. banks 2 and 3 on registered DIMM)
NC, FETEN	1	Reserved pin (FET enable)

Figure 4.5.10-C
184 PIN, 64, OR 72 BIT DDR SDRAM DIMM FEATURES &
PIN DESCRIPTIONS

184-Pin DDR SDRAM DIMM SPD Information

Notes:

The following information is to be written into EEPROM device during module production:

- a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	SDRAM Organization	SDRAM Density	Option 1 (primary)			Option 2		
			# Bank Addr.	RAS Addr.	CAS Addr.	# Bank Addr.	RAS Addr.	CAS Addr.
4M x 64/72	4M x 16	64Mb	2	12	8			
8M x 64/72	4M x 16	64Mb	2	12	8			
8M x 64/72	8M x 8	64Mb	2	12	9			
8M x 64/72	8M x 16	128Mb	2	12	9			
16M x 64/72	8M x 8	64Mb	2	12	9			
16M x 64/72	8M x 16	128Mb	2	12	9			
16M x 64/72	16M x 4	64Mb	2	12	10			
16M x 64/72	16M x 8	128Mb	2	12	10			
16M x 64/72	16M x 16	256Mb	2	13	9	2	12	10
32M x 64/72	16M x 8	128Mb	2	12	10			
32M x 64/72	16M x 16	256Mb	2	13	9	2	12	10
32M x 64/72	32M x 4	128Mb	2	12	11	2	13	10
32M x 64/72	32M x 8	256Mb	2	13	10			
32M x 64/72	32M x 16	512Mb		TBD				
64M x 64/72	32M x 8	256Mb	2	13	10			
64M x 64/72	32M x 16	512Mb		TBD				
64M x 64/72	64M x 4	256Mb	2	13	11			
64M x 64/72	64M x 8	512Mb		TBD				
64M x 64/72	64M x 16	1Gb		TBD				
128M x 64/72	64M x 8	512Mb		TBD				
128M x 64/72	64M x 16	1Gb		TBD				
128M x 64/72	128M x 4	512Mb		TBD				
128M x 64/72	128M x 8	1Gb		TBD				
256M x 64/72	128M x 8	1Gb		TBD				
256M x 64/72	256M x 4	1Gb		TBD				

Note: All options possible with SDRAM standards are shown.

- b. Allowable configurations: (Byte 11)
- x64 (Non-parity, Byte controls)
 - x72 (ECC-optimized, Byte controls)
- c. Functional Attributes:
- Power Supply Voltage/Interface levels (Byte 8)
 - SDRAM cycle time (Bytes 9, 23, 25)
 - SDRAM access from Clock (Bytes 10, 24, 26)
 - Refresh rate/type (Byte 12)
 - Primary/Secondary SDRAM width (Bytes 13, 14)
 - SDRAM device attributes (Bytes 15 - 20)
 - SDRAM module attributes (Bytes 21, 22)
 - SDRAM device timings (Bytes 27 - 30, 32 - 35)
 - Module bank density (Byte 31)
- d. Miscellaneous Information
- SPD revision (Byte 62)
 - Checksum (Byte 63)

Figure 4.5.10-D

184 PIN, 64, OR 72 BIT DDR SDRAM DIMM SPD INFORMATION

Pinout Comparison: 184 Pin Unbuffered DDR SDRAM to Unbuffered SDR SDRAM DIMM

Pin #	DDR DIMM	SDR DIMM
1	VREF	NU
5	DQS0	NU
14	DQS1	NU
17	CK1	NU
25	DQS2	NU
36	DQS3	NU
47	DQS8	NU
56	DQS4	NU
67	DQS5	NU
75	CK2	NU
78	DQS6	NU
86	DQS7	NU
97	DM0/DQS9	DQMB0
107	DM1/DQS10	DQMB1
119	DM2/DQS11	DQMB2
129	DM3/DQS12	DQMB3
138	CK0	NU
140	DM8/DQS17	DQMB8
149	DM4/DQS13	DQMB4
159	DM5/DQS14	DQMB5
169	DM6/DQS15	DQMB6
177	DM7/DQS16	DQMB7

Figure 4.5.10-E
184 PIN, 64, OR 72 BIT SDRAM DIMM DDR & SDR COMPARISON

Definition

The V_{DD} identification flag is a jumper connection on the DIMM which provides information on the relationship between V_{DD} and V_{DDQ} required by the memory devices on the DIMM. This jumper is installed on V_{DDID} on the DIMM as follows:

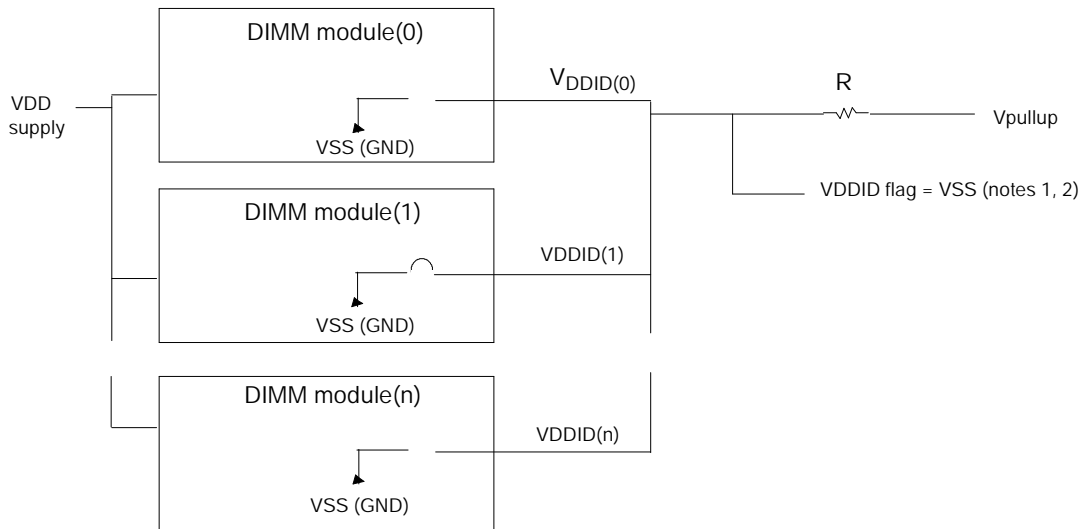
Device V_{DD} (nominal)	Device V_{DDQ} (nominal)	Jumper tied from V_{DDID} to
3.3 V	2.5 V	V_{SS}
2.5 V	2.5 V	Open
2.5 V	1.8 V	V_{SS}
1.8 V	1.8 V	Open
1.8 V	TBD	V_{SS}

Application

The V_{DDID} flag allows the system to detect the presence of DIMM modules for which memory device V_{DD} does not equal memory device V_{DDQ} . The system may then adjust the V_{DD} voltage.

Since this jumper is a V_{SS} connection, the module may be interrogated by the system without module V_{DD} or V_{DDQ} being on. The following two examples show how DIMMs may be connected to use this feature.

Example 1: DIMMs with VDD supplied to all sockets in common.

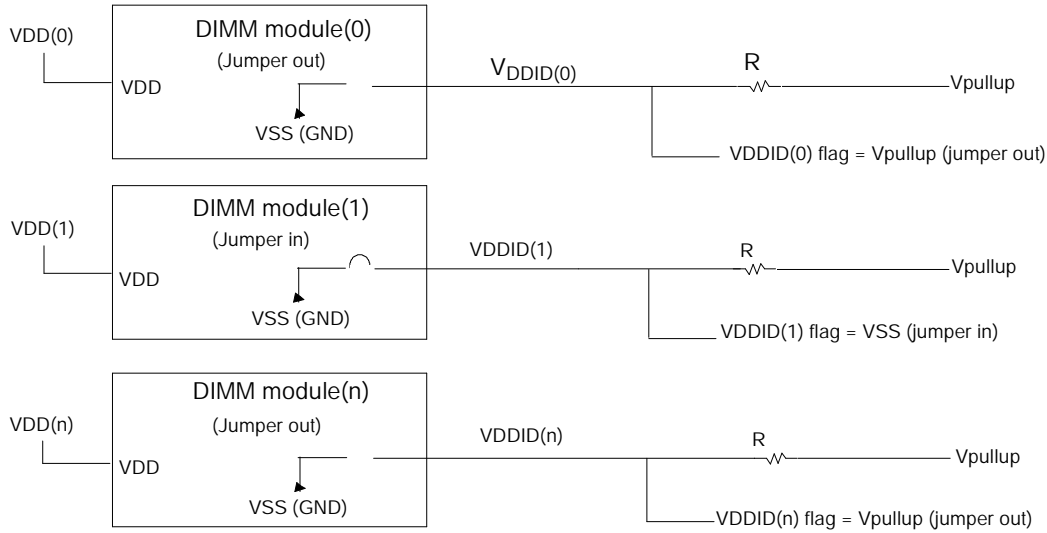


- a.**
1. In this example, DIMM module (1) is jumpered to V_{SS} and causes the combined flag to be at V_{SS} .
 2. Any position containing a DIMM with the jumper installed will cause the combined flag to be at V_{SS} .
 3. "R": Series resistor, nominally 1-10 kilohms.
 4. V_{pullup} may be 2.5 V or 3.3 V, but need not be related to V_{DD} or V_{DDQ} .

Figure 4.5.10-G
184 PIN, 64, OR 72 BIT SDRAM DIMM VDDID

Example 2: DIMMs with VDD supplied uniquely to each socket.

VDD may be adjusted for each DIMM, allowing DIMMs of different VDD but the same VDDQ to be used together.



Notes:

1. In this example, DIMM module (1) is jumpered to V_{SS}, causing only the the V_{DDID(1)} flag to be at V_{SS}. The others are at V_{pullup}.
2. "R": Series resistor, nominally 1 - 10 kilohms.
3. V_{pullup} may be 2.5 V or 3.3 V, but need not be related to V_{DD} or V_{DDQ}.

Figure 4.5.10-H
184 PIN, 64, OR 72 BIT SDRAM DIMM VDDID

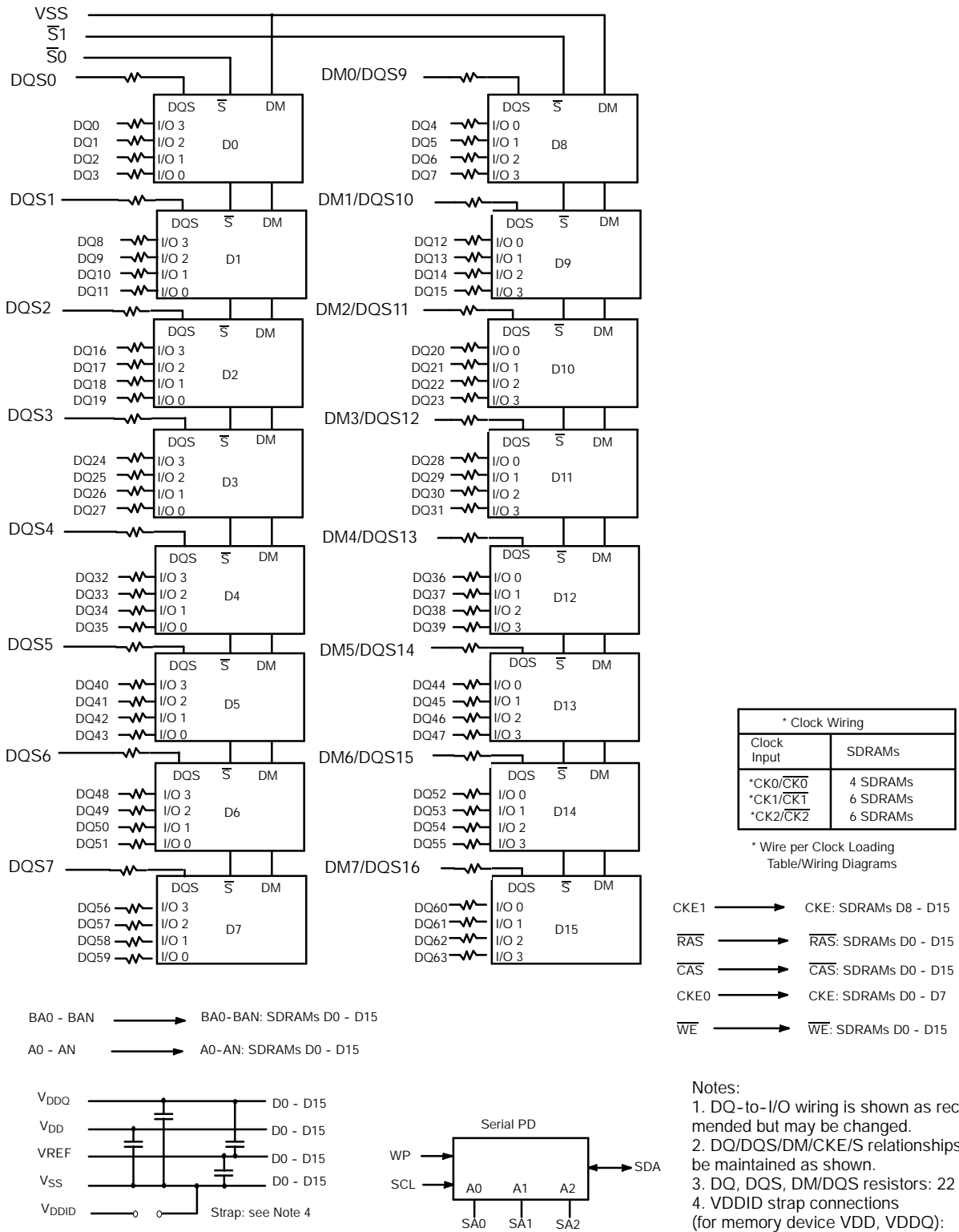


Figure 4.5.10-1

184 Pin, X64 DDR SDRAM DIMM, 1 Bank, X4 DDR SDRAMs

- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: 22 Ohms.
 4. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD + VDDQ.

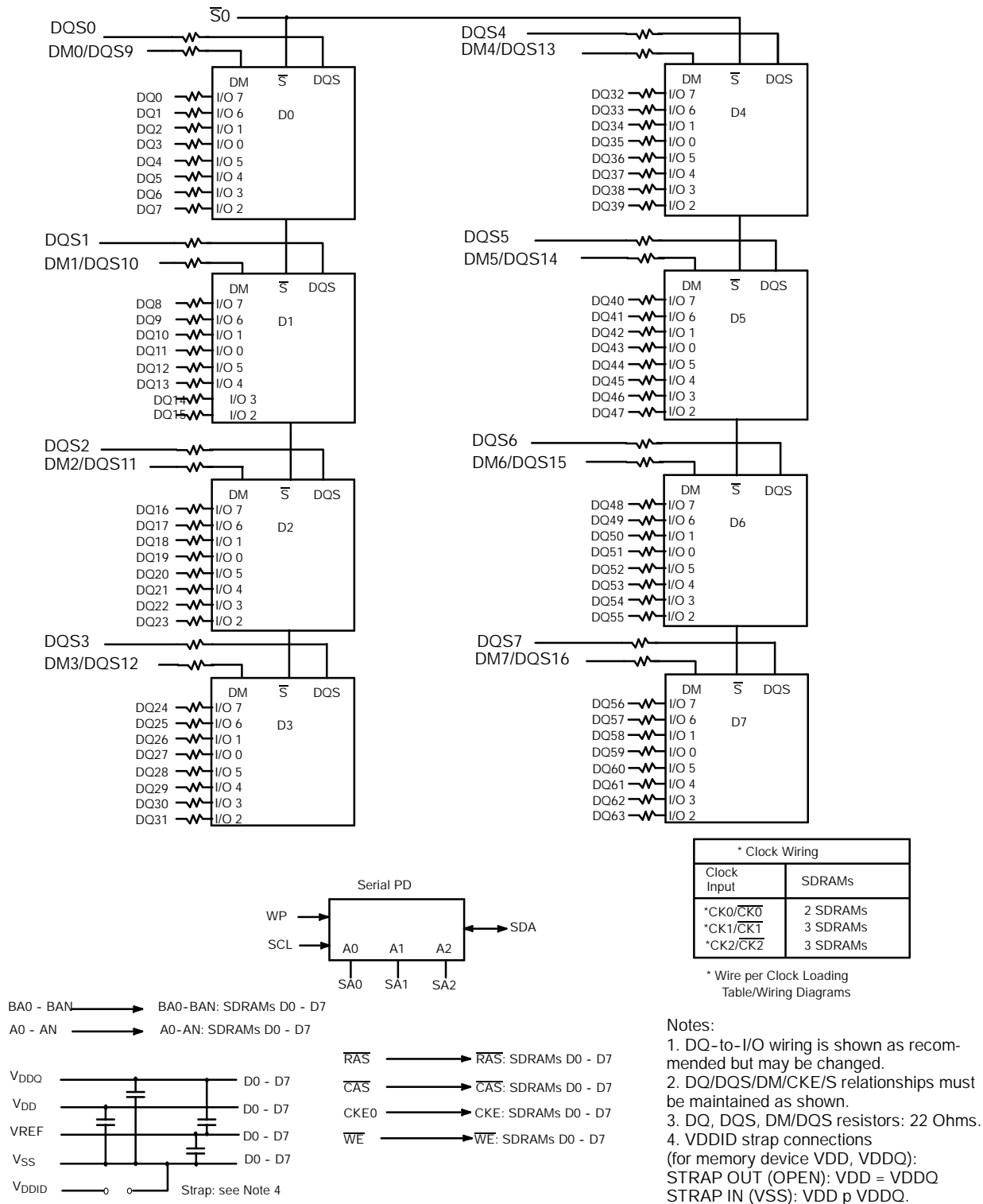


Figure 4.5.10-J
184 Pin, X64 DDR SDRAM DIMM, 1 Bank, X8 DDR SDRAMs
Release 9

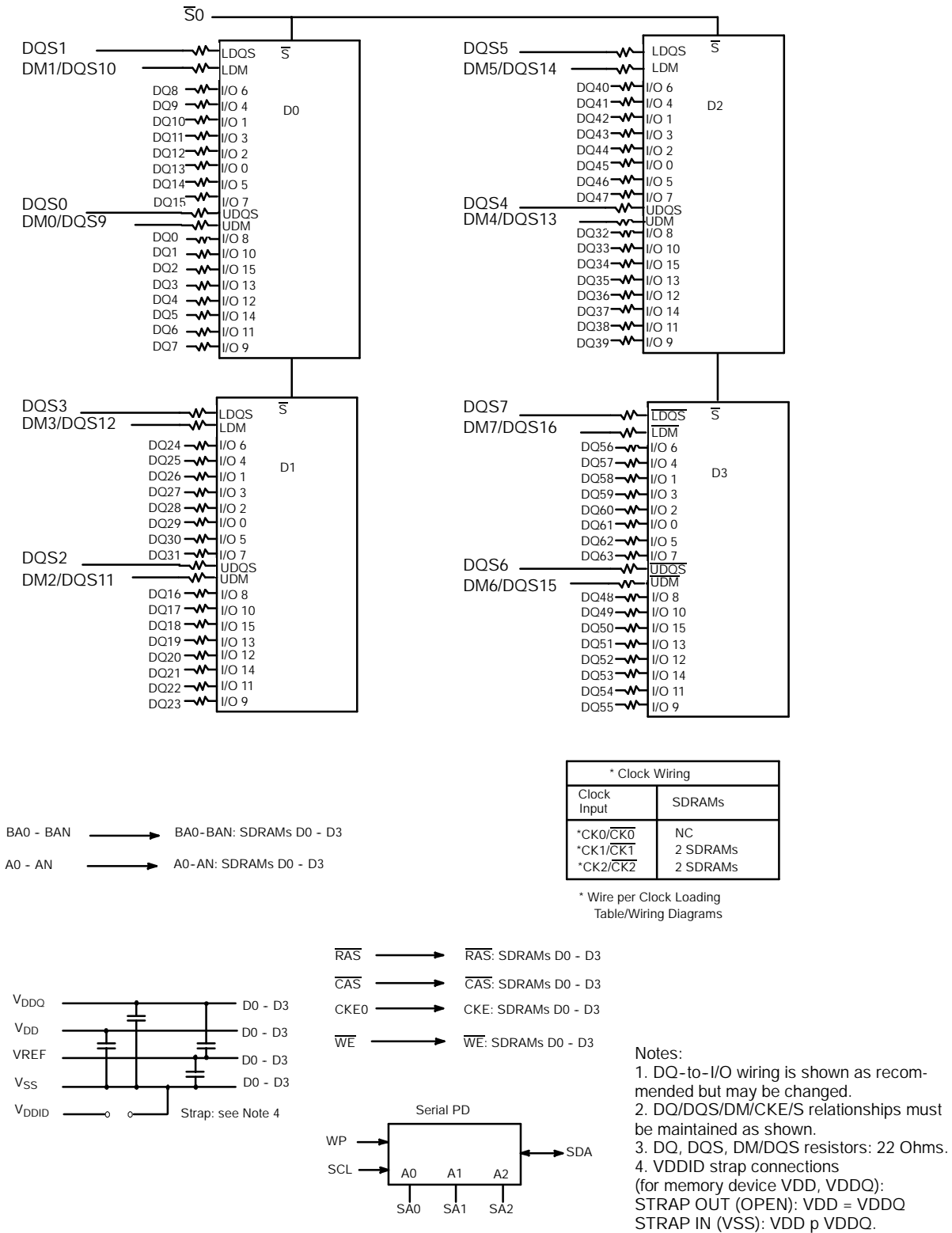


Figure 4.5.10-K
184 Pin, X64 DDR SDRAM DIMM, 1 Bank, X16 DDR SDRAMs

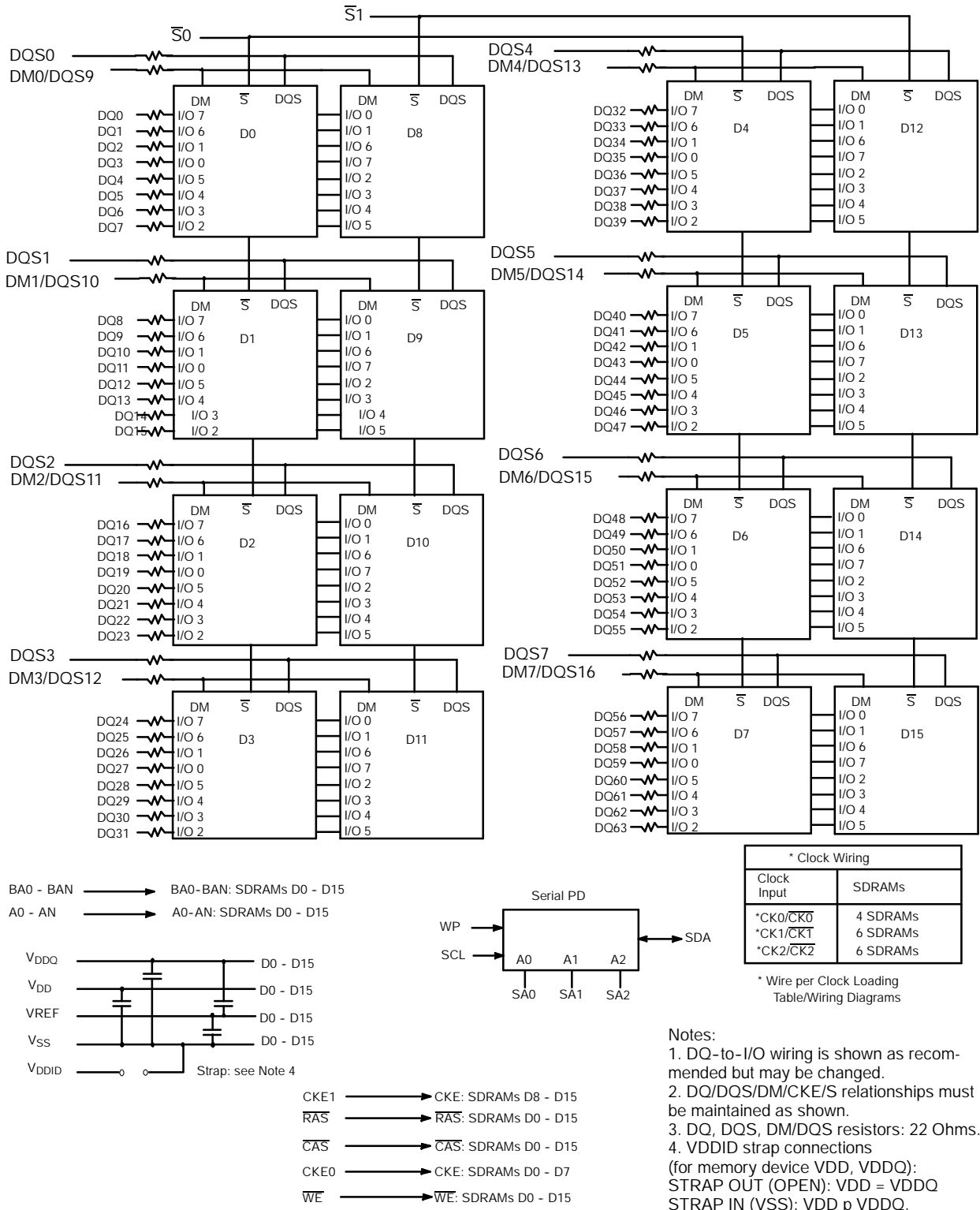
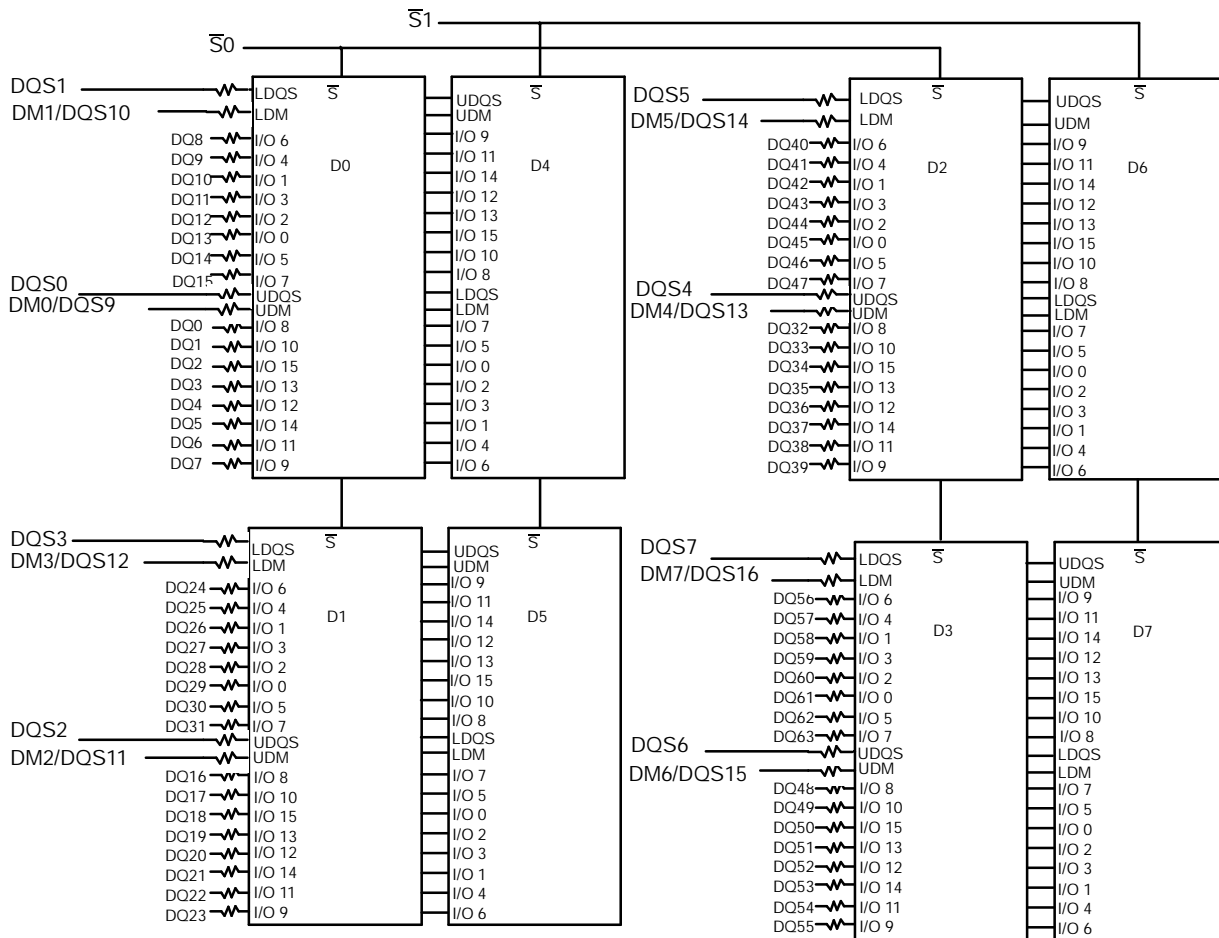


Figure 4.5.10-L
184 Pin, X64 DDR SDRAM DIMM, 2 Bank, X8 DDR SDRAMs
Release 9

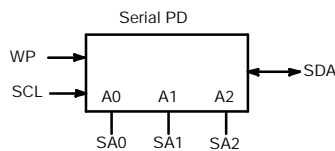
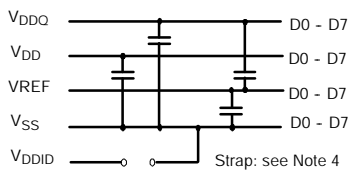


BA0 - BAN → BA0-BAN: SDRAMs D0 - D7
A0 - AN → A0-AN: SDRAMs D0 - D7

* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	NC
*CK1/CK1	4 SDRAMs
*CK2/CK2	4 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

CKE1 → CKE: SDRAMs D4 - D7
 \overline{RAS} → \overline{RAS} : SDRAMs D0 - D7
 \overline{CAS} → \overline{CAS} : SDRAMs D0 - D7
 CKE0 → CKE: SDRAMs D0 - D3
 \overline{WE} → \overline{WE} : SDRAMs D0 - D7



- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: 22 Ohms.
 4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD p VDDQ.

Figure 4.5.10-M
184 Pin, X64 DDR SDRAM DIMM, 2 Bank, X16 DDR SDRAMs

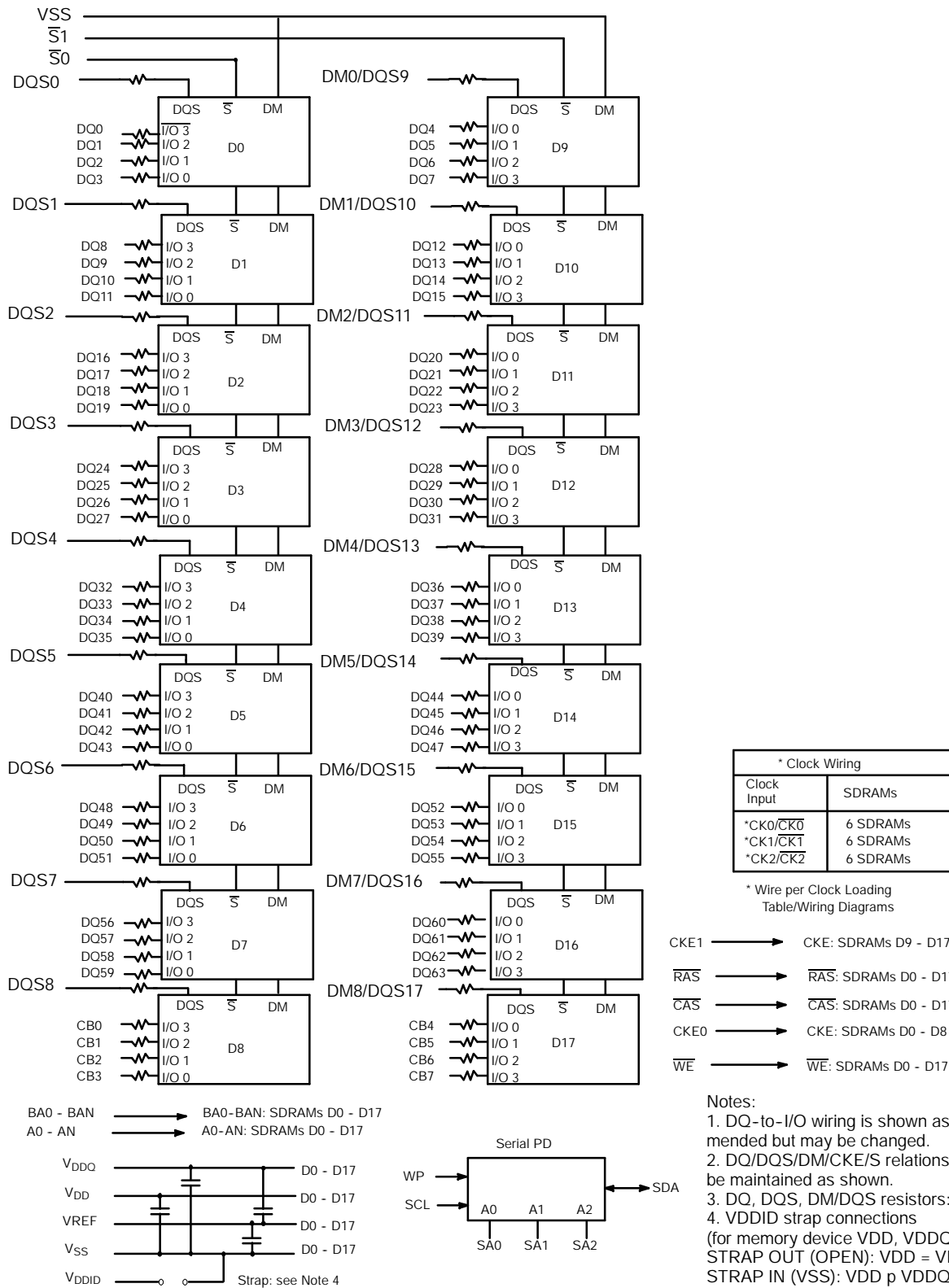
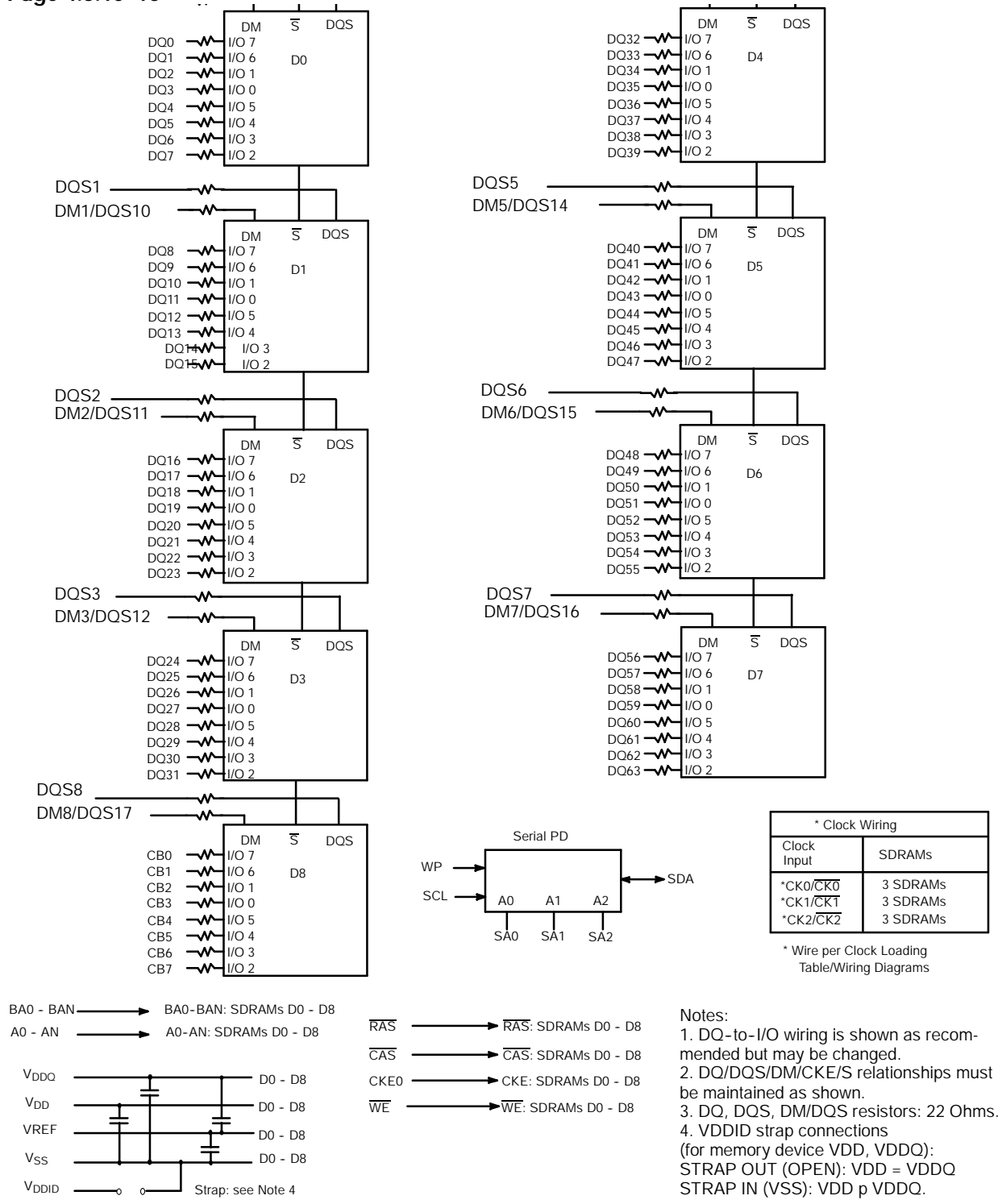
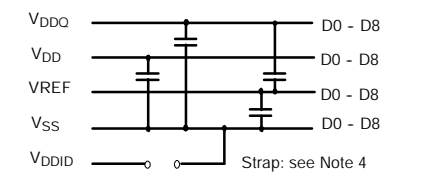


Figure 4.5.10-N
184 Pin, X72 ECC DDR SDRAM DIMM, 1 Bank, X4 DDR SDRAMs
Release 9



BA0 - BAN → BA0-BAN: SDRAMs D0 - D8
A0 - AN → A0-AN: SDRAMs D0 - D8



\overline{RAS} → \overline{RAS} : SDRAMs D0 - D8
 \overline{CAS} → \overline{CAS} : SDRAMs D0 - D8
CKE0 → CKE: SDRAMs D0 - D8
 \overline{WE} → \overline{WE} : SDRAMs D0 - D8

Figure 4.5.10-O

184 Pin, X72 ECC DDR SDRAM DIMM, 1 Bank, X8 DDR SDRAMs

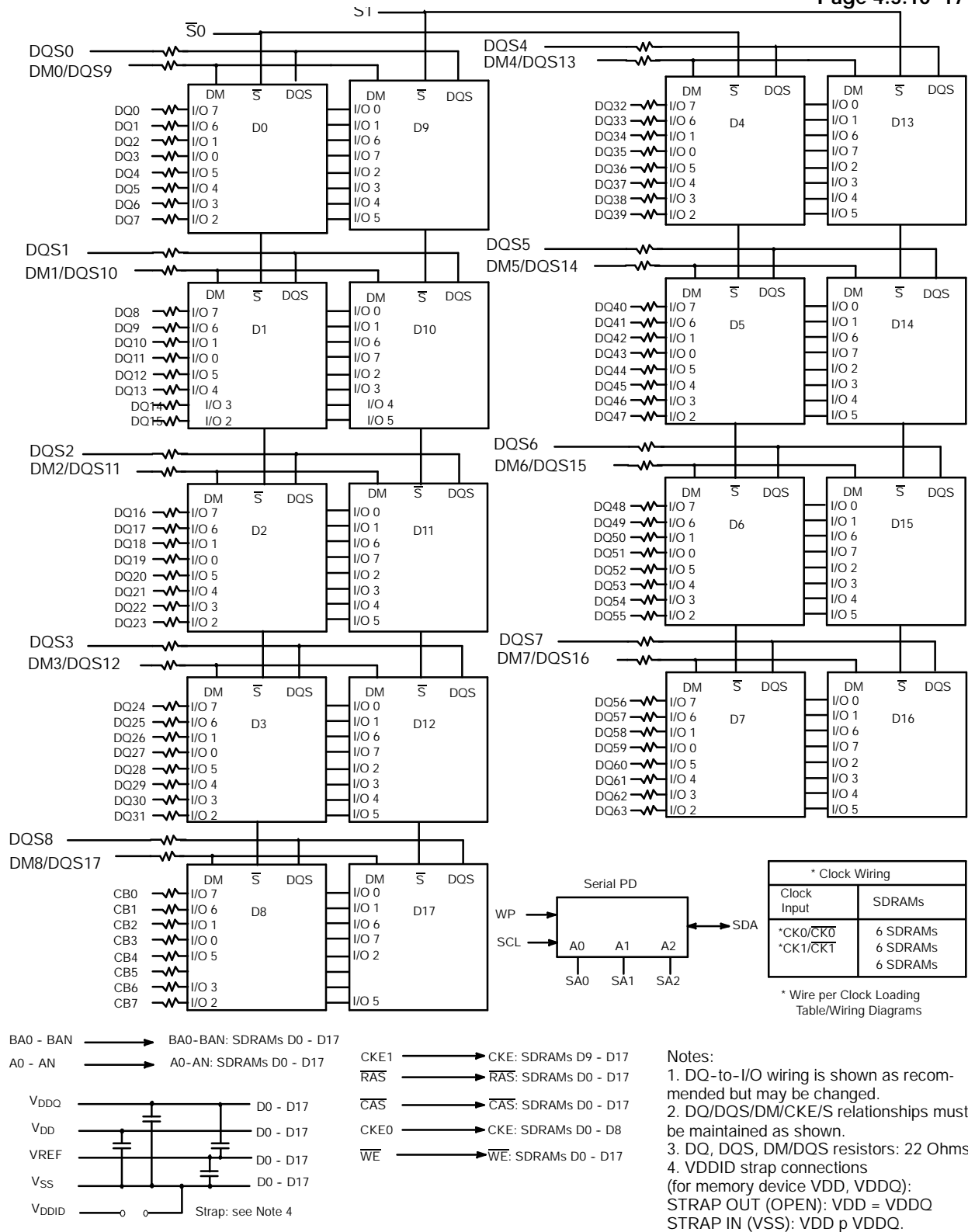


Figure 4.5.10-P
184 Pin, X72 ECC DDR SDRAM DIMM, 2 Bank, X8 DDR SDRAMs
Release 9